REMARKS

In the Office Action dated September 16, 2003, claims 1-16 are noted as pending. Claims 1-9 and 15-16 are rejected under 35 USC 102(b) as being anticipated by Saulsbury et al., U.S. Patent No. 6,128,702 (hereinafter Sualsbury). Claims 10-14 are rejected under 35 USC 103(a) as being unpatentable over Westberg et al., U.S. Patent No. 5,361,391 (hereinafter Westberg) in view of Saulsbury.

Objections to the Specification

The specification has been amended to cure the informality.

REJECTIONS UNDER 35 U.S.C. 102(b)

Saulsbury does not disclose a data cache located on a memory module controlled by a command sequencer and serializer unit where the "command sequencer and serializer unit to reduce a first plurality of address and command signals down to a more narrow set of signal lines coupled to the memory module, the more narrow set of signal lines forming a point-to-point interconnect between the command sequencer and serializer unit and the memory module" as claimed in amended claim 1. It should be noted that the command sequence and serializer unit and array of tag addresses are not located on the memory module, as indicated by the language of claim one describing an interconnect coupling the command sequencer and serializer unit to the memory module. The tag array, data cache, and memory bank in Saulsbury are all located on the same

component, and there is no teaching of a serializer unit with the limitations claimed in claim 1. For these reasons, claim 1 is distinguished over Saulsbury.

Similarly, Saulsbury does not disclose a memory module including a data cache that is controlled by a memory controller including an array of tags where the memory controller is not located on the memory module, as claimed in amended claim 7.

Further, Saulsbury does not disclose, as claimed in claim 15,

> "performing a tag look-up within the memory controller to determine whether there is a cache hit for the read request; and
> fetching a line of cache data from a data cache located on a memory module if the tag look-up indicates a cache hit, the memory module separate from the memory controller and coupled to the memory controller via a memory bus."
> (amended claim 15, emphasis added)

For these reasons, claims 1-9 and 15-16 are distinguished over Saulsbury.

REJECTIONS UNDER 35 U.S.C. 103(a)

Neither Westberg nor Saulsbury, either alone or in combination, disclose a memory controller including an array of tag address locations coupled to a memory module via a memory bus where the memory module includes a data cache controlled by the memory controller, as claimed in amended claim 10. Therefore, claims 10-14 are patentable over Westberg in view of Saulsbury.

CONCLUSION:

In view of the foregoing, Applicants submit that claims 1-16 are distinguished over the cited art and are in condition for allowance. Allowance of claims 1-16 is respectfully requested.

DEPOSIT ACCOUNT AUTHORIZATION

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any additional charges that may be due.

Respectfully submitted,

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Dated: December 31, 2003

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